



White Paper

# End-use Applications for Multicore Processors

FreescalQorIQ™ Communications  
Platform P1, P2 and P4 Series

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## Overview

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The newest processors in Freescale Semiconductor's next-generation Multicore Communications Platform cover a range of applications, from low-end routers for small and medium businesses to complex network management. This paper provides details and diagrams for five example applications that can be enabled by Freescale's QorIQ™ communications platform P1, P2 and P4 Series processors.

Freescale QorIQ communications platforms are the next-generation evolution of our leading PowerQUICC® communications processors. Built using high-performance Power Architecture® cores, Freescale QorIQ platforms enable a new era of networking innovation where the reliability, security and quality of service for every connection matters.

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# 1 Introduction to QorIQ Communications Processors

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Freescal Semiconductor's QorIQ™ communications platform P1, P2 and P4 series processors are the newest processors in the next-generation Multicore Communications Platform. Each processor in the series is designed for 45nm technology to deliver networking services in a very low power envelope.

The **QorIQ P1 platform series**, which includes the P1020, P1011 and P1010 communications processors, supports a wide variety of applications in the networking, telecom, military and industrial markets. The series provides dual and single core solutions for the 400 MHz to 800 MHz performance range, along with advanced security and a rich set of interfaces. The P1 platform series is suited for multiservice gateways, Ethernet switch controllers, wireless LAN access points, and high-performance general-purpose control processor applications with tight thermal constraints.

The **QorIQ P2 platform series**, which includes the P2020 and P2010 communications processors, delivers unprecedented performance per watt for a wide variety of applications in the networking, telecom, military and industrial markets. The series delivers dual- and single-core frequencies from 800 MHz to 1.2 GHz.

The QorIQ P2 series consists of dual- and single-core products that are pin-compatible with the QorIQ P1 platform products, offering five interchangeable cost-effective solutions. Scaling from a single core at 400 MHz (P1010) to a dual core at 1.2 GHz (P2020), the two QorIQ platforms together deliver an impressive 6x aggregate frequency range within the same pinout.

The devices in the P1 and P2 series are also software compatible, sharing the e500 Power Architecture core and peripherals, as well as being fully software compatible with the existing PowerQUICC® processors. This enables you to create a product with multiple performance points from a single board design.

The **QorIQ P4 platform series'** first processor is the QorIQ P4080 multicore processor, which delivers industry-leading performance in the under 30-watt power category. It combines eight Power Architecture® e500mc cores—operating at frequencies up to 1.5 GHz—with high-performance datapath acceleration logic, as well as networking I/O and other peripheral bus interfaces.

The QorIQ P4080 processor is designed for combined control and dataplane processing, enabling high-performance Layer 2–7 processing. Its high level of integration offers significant performance benefits compared to multiple discrete devices, while also greatly simplifying board design. This makes it ideal for applications such as enterprise and service provider routers, switches, base-station controllers, radio network controllers (RNCs), access gateways for Long Term Evolution (LTE) and general-purpose embedded computing systems in the networking, telecom, industrial, military and aerospace markets.

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## 2 Small and Medium Business/Branch Office Router

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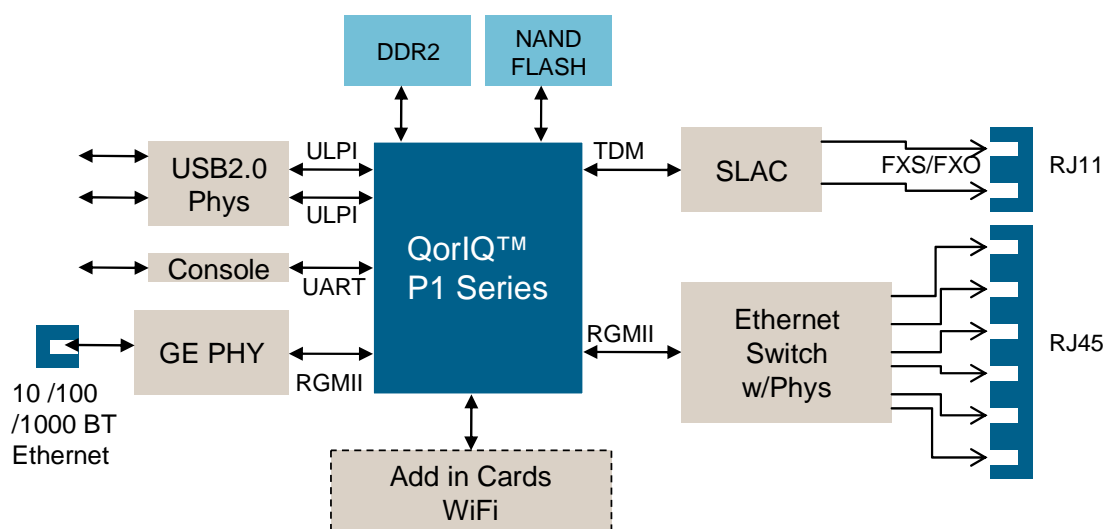
Most OEMs build a range of router products to offer scalable solutions that meet the needs of different sizes of businesses and different service delivery options. The ideal processor choice for this application is a pin- and software-compatible family of devices that can provide hardware reuse and scalable performance to deliver different performance and service options.

Typically a small business requires a simple, easy to deploy solution that can grow as the business grows. Because local IT support for these businesses may be limited, solutions must work out of the box and be easy to manage and troubleshoot. Upgrading firmware or adding new services remotely must also be simple. In many cases these routers integrate a full router, Ethernet switch, security and IP-PBX in a single unified communications platform. All these services and applications require a high-performance scalable architecture such as that provided by Freescale's QorIQ™ P1 and P2 series of processors, which scale from 400 MHz single core to 1.2 GHz dual-core.

The QorIQ P1 and P2 series of processors can meet several important technical challenges in this market, including:

- Scalability in performance and cost to support different numbers of users
- Low-power operation
  - Simplified thermal design
  - Fanless design for higher reliability
- Flexibility to enable multiple product derivatives using a single pin-compatible hardware platform, differentiated by software

**Figure 2.1. Example SMB/branch office router using Freescale's QorIQ P1 series processors**



The features illustrated in Figure 2.1 include:

- Dual-core asymmetric multiprocessor (AMP) support
- One core for services and one for applications
- High-performance routing
- Security
  - Network address and port translation (NAPT) and firewall
  - Encrypted VPN
- Wireless 802.11N with option card
- VoIP through SIP proxy and TDM
  - SIP phones
  - Analog phones
  - PSTN failover (lifeline)

### 3 Enterprise/WLAN Access Point

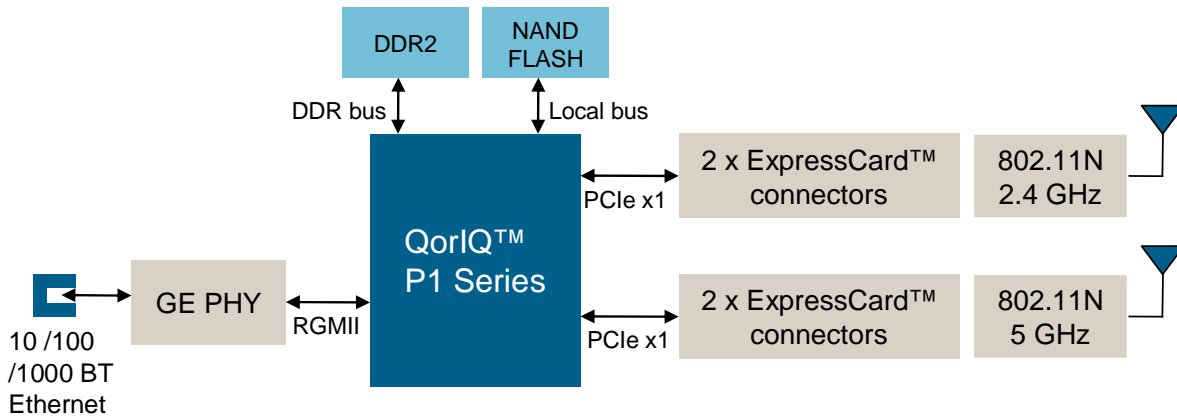
A primary application for Freescale's QorIQ P1 series of processors is the enterprise wireless LAN access point market. These applications are well-suited to our approach of combining high-performance and lower power processors with the required I/O to minimize external components and system cost.

Typically, enterprise WLAN access points support a single triple-speed Ethernet port that connects to an Ethernet switch. The access point may be powered directly from the Ethernet switch if it supports power over Ethernet (PoE), or

it may be powered from an external source. In the case of PoE the IEEE® 802.3af class 3 specifies maximum power of 12.95W. Freescale's QorIQ P1 series enables high-performance enterprise class solutions with low-power operation.

With the IEEE 802.11n standard, wireless technology can now provide the same levels of performance as wired infrastructure, and can replace the wired infrastructure in new deployments.

**Figure 3.1. Example enterprise/WLAN access point using Freescale's QorIQ P1 series processors**



Challenges that the QorIQ P1 series meets in these applications include:

- IEEE 802.3af PoE standard limits restrict the amount of power that can be delivered, mandating high performance at low power
- Performance
  - IEEE 802.11n increases throughput to the level of wired installations
  - Trend towards increased throughput with more radios (4 x 4)
- Quality of service (QoS) required to support VoIP over Wi-Fi for enterprise applications

## 4 LTE and WiMAX Baseband Applications

Two processors in Freescale's QorIQ P2 Series, the P2020 and P2010 communications processors, are well-suited for Long Term Evolution (LTE) and WiMax channel card applications. There are two factors that drive the need for dual core performance without breaking out of a single-core power budget. The first is increased bandwidth per subscriber and the second is the flattening of the infrastructure hierarchy, which greatly increases the processing requirements at the channel card. The two primary functions that need increased performance are Layer 2 baseband processing and implementing network interfaces.

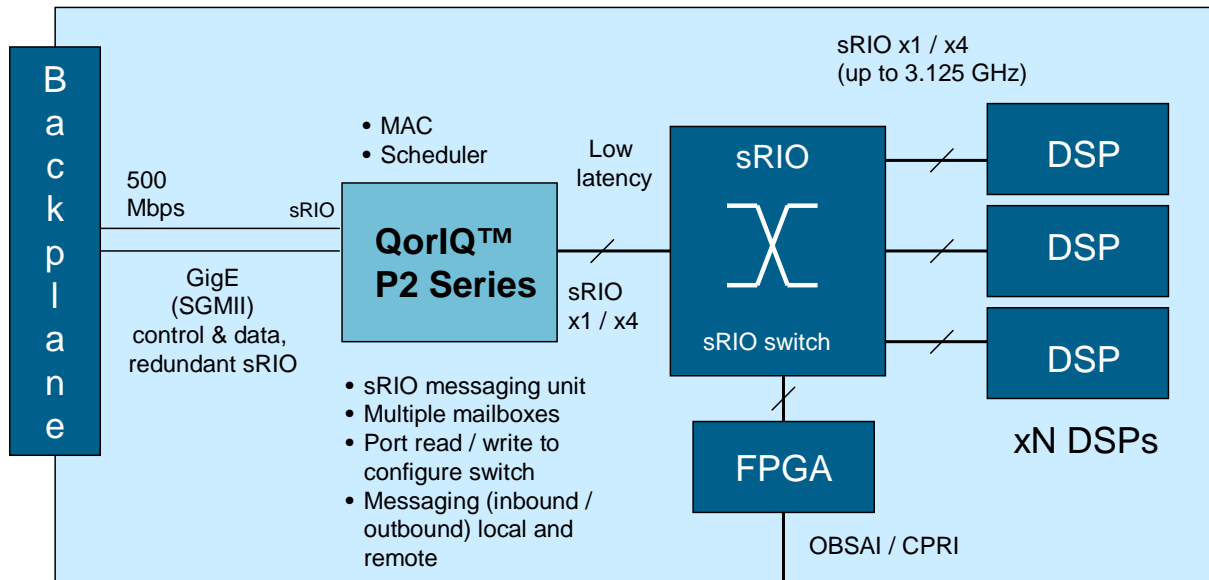
Layer 2 baseband processing implements the RLC layer that controls the base station and subscriber access to air interface resources. The advanced QoS features of the Gigabit Ethernet ports assist in scheduling these resources. This Layer 2 processing includes the Medium Access Control (MAC), which controls the base station and subscriber access to air interface resources. Resources are scheduled according to QoS requirements using packet concatenation and segmentation, retransmission through automatic repeat request (ARQ) and hybrid automatic repeat request (HARQ) in combination with Layer 1.

Typically backhaul is implemented with either dual Gigabit Ethernet on SGMII (for redundancy) or Serial RapidIO interface, both of which are supported in the QorIQ P2 series processors. The Serial Rapid IO interface also allows direct connection to the digital signal processors (DSPs)—such as Freescale's MSC8144 Quad-Core DSP—that implement the Layer 1 processing. The security block handles the secure network termination requirement.

This solution performs network backhaul transport and interworking with internal interfaces. This includes processing the network layers up to OSI Layer 3, including IPsec secure network termination, header compression and traffic

classification (QoS). The Network Interface Card (NIC) can optionally support 3G LTE radio link encryption—however, depending upon the selected architecture, this could be partitioned to the channel card.

**Figure 4.1. Example channel card application using Freescale's QorIQ P2 series processors**

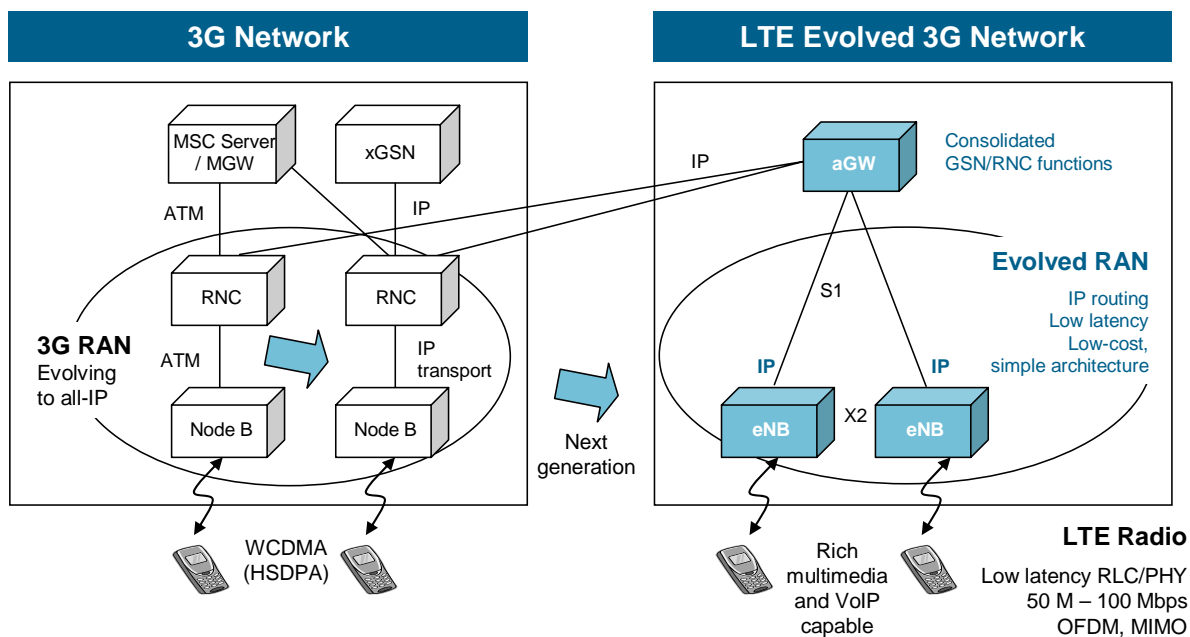


#### 4.1 Enabling Improved Architectures

In addition to data-rate increases, there are other technology challenges that this next generation equipment must deliver to offer additional cost and mass scaling efficiencies versus existing technologies.

Figure 4.2 illustrates several technology challenges that the evolution from 3G to LTE presents. Table 4.1 outlines the associated Freescale base station platform solutions to those challenges.

**Figure 4.2. Network architecture evolution from 3G to LTE**



**Table 4.1. Processor challenges in the evolution from 3G to LTE**

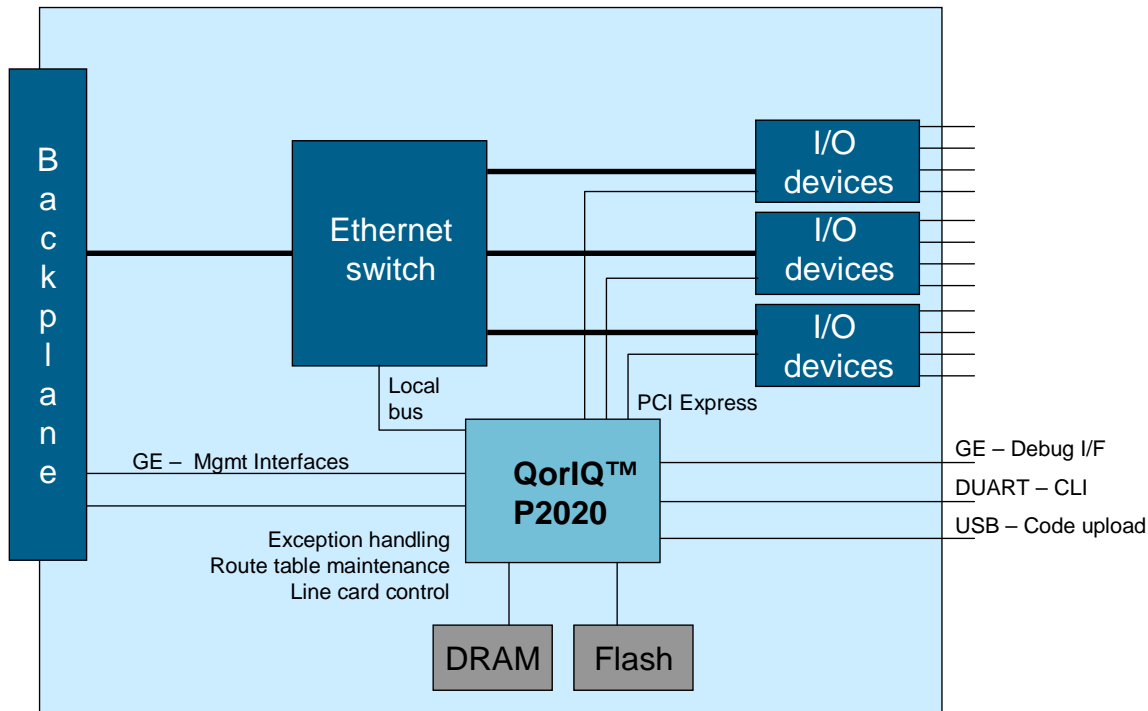
	Existing 3G	LTE requirement	Impact on processor
<b>User data-rate (per sector)</b>	~300kbps – 14Mbps	> 100Mb/s	Increased processing
<b>Latency</b>	50 ms (Rel6) Example: web browsing	10 ms (Rel8) Example: VoIP, gaming	Integration
<b>Hierarchies</b>	Three	Two – lower latency, cost	Higher processing densities in same power budget
<b>Protocols in NodeB (Non-L1)</b>	Control, scheduler	Radio bearer, control, radio admission control, dynamic scheduler, inter cell radio resource management, connection mobility control, NodeB measurement, configuration and provision, RRC, PDCP, RLC, MAC	Intelligence required

Besides the obvious performance impact of more bandwidth per subscriber, the collapse from three levels of hierarchy to two levels affects the processor on the NodeB as well. The reason for the collapse is largely because of the need to decrease user latency in order to enable more interactive applications. As a result, functions that previously were performed by high-power processors in the RNC are now performed at the NodeB, which retains its very slim power budget. This combination of high performance with low power budget makes the P2 family a perfect match.

## 5 Line Card Control Plane

One of the primary applications for the Freescale QorIQ P2020 communications processor is as a line card control plane processor. Typically the P2020 will sit to the side of the main datapath, which has I/O processors on the front panel connected to a backplane interface device. The P2020 will communicate with these components using standard interfaces such as PCI Express or the local bus. The P2020 will often have front panel interfaces as well. One Gigabit Ethernet interface may be used for high-performance debug; the DUART can be used for a low-level command line interface; and the USB port may be used for front-panel code uploads when connecting directly to a PC for maintenance. Redundant Gigabit Ethernet ports to the backplane are used as a management interface, which can be used to communicate with a centralized resource for receiving table updates, for instance. The SD/MMC interface enables modularity by supporting booting from Flash cards.

**Figure 5.1. Example line card control plane application using Freescale's QorIQ P2020 processor**



The primary functions of a linecard controller are:

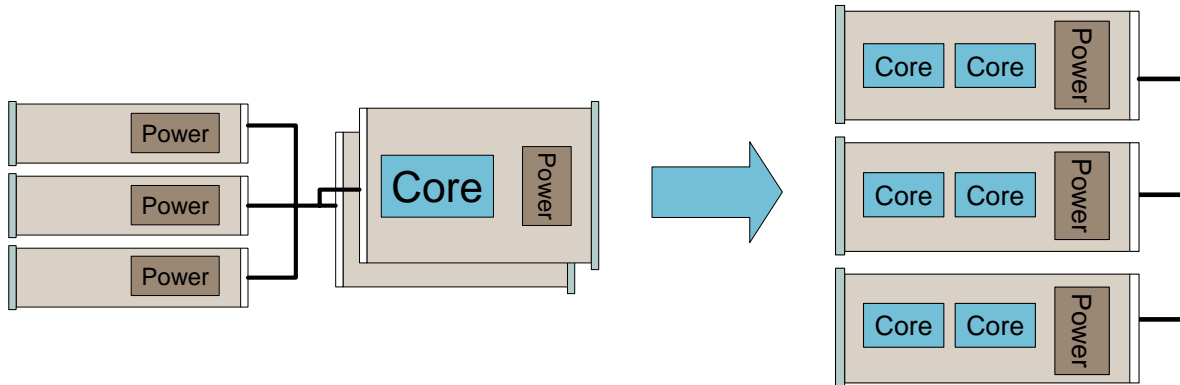
- **Exception handling.** Packets that cannot be interpreted by the typically more hardwired datapath are kicked up to the control plane processor. These may be older or esoteric protocols which are not worth accommodating in ASICs, but can be handled with software with low performance impact because they occur infrequently.
- **Board housekeeping.** The control plane processor may be used to configure, provision and control other devices on the board. It also will collect statistics. It can implement a command line interface.
- **Table maintenance.** A line card controller may, especially in a distributed system, manage the forwarding tables. The tables are created by implementing a variety of interior routing protocols (such as Open Shortest Path First or Routing Information Protocol) and external routing protocols (such as Border Gateway Protocol). The tables are then exported to the forwarding path for per-packet access.

In the case of centralized processing, these functions are performed by a centralized processor, which can tolerate a higher power and associated increased cooling costs because there are fewer of those cards per system. In these cases, the line card has little intelligence.

Implementing a line card in a distributed processing system provides several advantages. You may be able to forgo the costly centralized services card, which consumes a valuable slot in the chassis. You have the opportunity to perform local switching at the line card, thus conserving system resources. And the system becomes more scalable—as you add a line card, you automatically get the increased processing it that requires. However, in this system, the costs of high-volume line cards are critically important. Because of that, thermal budgets are very tight. The high performance at low power is a requirement that the P2 family meets.



**Figure 5.2. QorIQ processors allow implementation of a distributed processing system that meets power/performance requirements**



## 6 VPN/IP Services Router

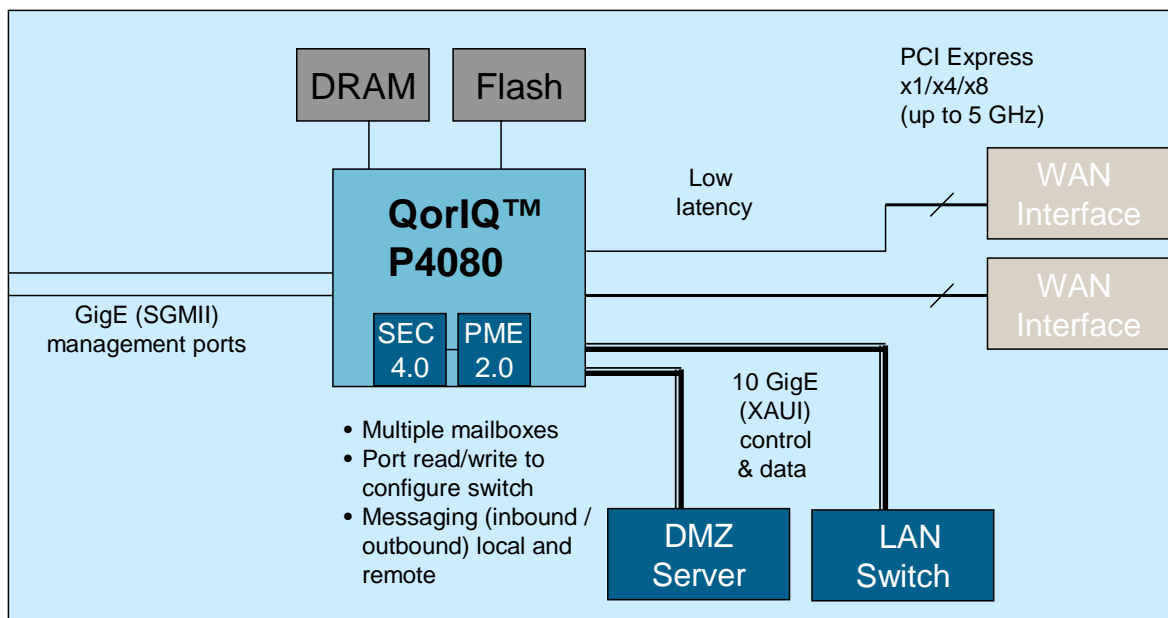
VPNs remain one of the most important pieces of network security equipment in most enterprises. There is a trend in network security towards application content security, higher integration and higher speed. The eight-core QorIQ P4080 multicore processor excels at providing the processing power for advanced content processing and security features.


Figure 6.1 shows a virtual private network (VPN)/IP Services router enabled through PCI-Express™ expansion card and Ethernet interconnections. For this type of application, an eight-core processor provides the following benefits:

- Overall high rate of speed to process large quantities of data
- Flexibility to work in Asymmetric Multi-Processing (AMP) or Symmetric Multi-Processing (SMP) modes
- Ability to manage keys and set up to tunnel data

Extra cores also allow a company to grow from a four-port VPN to manage more ports, and to potentially add services such as a firewall or stateful deep packet inspection.

**Figure 6.1. Example of a VPN/IP services router using the Freescale QorIQ P4080 processor**





The QorIQ P4080 Datapath Acceleration Architecture accelerates packet classification, filtering, and packet queuing, while the crypto accelerator (SEC 4.0) and Pattern Matching Engine (PME 2.0) perform high-throughput encryption/decryption and Regular Expression (RegEx) packet payload scanning security under control of stacks running on the cores in the P4080. The SEC 4.0 block is responsible for IPSec tunneling and private key management.

The SEC 4.0 is the fourth generation of the security block, and is the first to be included in the QorIQ P4080. The SEC 4.0 includes five Descriptor Controllers (DECOs), which are updated versions of the previous SEC crypto-channels. DECOs are responsible for header and trailer processing, and managing context and data flow into the CHAs assigned to it for the length of an operation. The DECOs can perform header and trailer processing, as well as single-pass encryption/integrity checking for the following security protocols:

- IPSec
- Secure Sockets Layer (SSL)/Transport Layer Security (TLS)
- Secure Real-time Transport Protocol (SRTP)
- IEEE 802.1AE Media Access Control Security (MACSec)
- IEEE 802.16e WiMAX MAC layer
- 3GPP RLC encryption/decryption

Security execution units on the QorIQ P4080 are referred to as Crypto Hardware Accelerators (CHAs) to distinguish them from prior implementations. Specific SEC 4.0 CHAs available to the DECOs are:

- Advanced Encryption Standard unit (AESA)
- ARC four execution unit (AFHA)
- Cyclic Redundancy Check Accelerator (CRCA)
- Data Encryption Standard execution unit (DESA)
- Kasumi execution unit (KFHA)
- SNOW 3G Hardware Accelerator (STHA)
- Message digest execution unit (MDHA)
- Public key execution unit (PKHA)
- Random number generator (RNGB)

Depending on the security protocol and specific algorithms, the SEC 4.0 blocks aggregate symmetric encryption/integrity performance will be 10 Gbps, while asymmetric encryption (RSA public key) performance will be approximately 10,000 1024b RSA operations per second.

Session establishment, policy enforcement, and potentially application processing are executed by the P4080's control processor(s).

In a different application, security appliances would use the QorIQ P4080 in a similar manner. However, they would not have direct connections to the WAN and demilitarized zone (DMZ) server.

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